AF
JFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

DAVID L. LARKIN ET AL.

Serial No. 09/988,651 (TI-23422.1)

Filed November 20, 2001

For: A METHOD FOR DECREASING CHC DEGRADATION

Art Unit 2891

Examiner Igwe U. Anya

Customer No. 23494

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING OR TRANSMISSION UNDER 37 CFR 1.8

I hereby certify that the attached document is being deposited with the United States Postal Service with sufficient postage for First Class Mail in an envelope addressed to Director of the United States Patent and Trademark Office, P.O. Box 1450,, Alexandria, VA 22313-1450 or is being facsimile transmitted on the date indicated below:

6-2-06

Jay M. Cantor, Reg. No. 19,906

Sir:

BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences.

STATUS OF CLAIMS

This is an appeal of claims 12 to 14, 20 to 23 and 29, all of the rejected claims. Claims 1 to 11, which are the subject of Patent No. 6,350,673, have been canceled and claims 15 to 19 and 24 to 28 have been indicated to be allowable if rewritten in independent form. Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

An amendment was filed after final rejection and not entered.

SUMMARY OF CLAIMED SUBJECT MATTER

The claimed invention relates to a method of decreasing channel hot carrier (CHC) degradation in semiconductor devices. This problem is minimized in accordance with the present invention, as stated in claim 12, by providing a semiconductor device manufactured using the process of providing a semiconductor device having at least one metal layer completed, then applying a planarizing dielectric layer on top of the semiconductor device and the metal layer and then providing a hydrogen treatment until hydrogen diffuses throughout and substantially saturates the semiconductor device. The term "substantially" is used since it is possible and even likely that an insignificant number of sites may not be saturated with the hydrogen.

The hydrogen treatment can include heating the semiconductor device in a hydrogen rich environment or applying hydrogen in situ by introducing hydrogen as a plasma to the semiconductor device. The semiconductor device can undergoe the hydrogen treatment after a final layer of the planarizing dielectric layer is added.

In accordance with claim 21, the semiconductor device is manufactured by providing a semiconductor device having thereon at least one metal layer completed and then providing a hydrogen treatment until hydrogen diffuses throughout and substantially saturates the semiconductor device. The hydrogen treatment can include heating the semiconductor device in a hydrogen environment or applying hydrogen in situ by introducing hydrogen as a plasma to the semiconductor device.

GROUNDS OF REJECTION

Claims 12 to 29 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

Claim 12, 20, 21 and 29 were rejected under 35 U.S.C. 102(e) as being anticipated by Ino et al. (U.S. 5,888,839).

Claim 12 to 14 and 21 were rejected under 35 U.S.C. 102(b) as being anticipated by Mora (U.S. 4,920,077).

ARGUMENT

Claims 12 to 29 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite. The rejection is without merit. In this regard, reference is made to M.P.E.P. 2173(c) D wherein the term "substantially" is stated by Court decision not to be indefinite. Furthermore, it is not indefinite in the sense used in the present claims. The intent is to totally saturate the device with hydrogen. However, it is possible and probably likely to a very small and insignificant number of sites may be unsaturated without in any way altering the invention herein. Such devices are also covered by the invention herein and the term "substantially" is used to cover such devices.

Claim 12, 20, 21 and 29 were rejected under 35 U.S.C. 102(b) as being anticipated by Ino et al. (U.S. 5,888,839). The rejection is without merit.

Claim 12 requires, among other features, the steps of applying a planarizing dielectric layer on top of the semiconductor device and the metal layer; and then providing a hydrogen treatment until hydrogen diffuses throughout *and substantially saturates the semiconductor device*. No such steps are taught or even remotely suggested by Ino et al. Ino et al. provide the hydrogen for an entirely different purpose and, more importantly, do not diffuse the hydrogen throughout and substantially saturating the semiconductor device. The treatment in accordance with the present invention will either pacify any dangling bonds in the semiconductor device to prevent damage to the gate oxide layer or cause the hydrogen to bond with contaminants, thereby making the contaminant too large to diffuse through the semiconductor device. No such treatment is taught or even remotely suggested by Ino et al. There is clearly no teaching or suggestion in Ino et al. to saturate the semiconductor device with hydrogen.

In the Advisory Action, the examiner has now, for the first time, cited the Miyazaki (U.S. 6,335,278). This patent has nothing whatsoever to do with the problem of decreasing CHC degradation or of saturating a semiconductor device with hydrogen for this purpose. While, even if it were known that semiconductor devices could be saturated with hydrogen, there would be no reasons to believe and clearly no teaching to use such method to decrease CHC degradation.

The above features are also found in claim 21. In addition, claims 13 14, 20, 22, 23 and 29 depend from one of claims 12 and 21 and therefore define patentably over Ino et al. for at least the reasons presented above with reference to claim 12.

Claims 12 to 14 and 21 to 23 were rejected under 35 U.S.C. 102(b) as being anticipated by Mora (U.S. 4,920,077). The rejection is without merit.

With reference to claims 12 and 21, the argument presented above with reference to Ino et al. applies as well in this case and is incorporated by reference.

The examiner refers to column 4, lines 48-54 of Mora for heating in a hydrogen-rich atmospherel Mora fails for at least two reasons. The first, as stated above, is that there is no teaching or suggestion that hydrogen is used to *saturate* the device as required and there is no saturation for the purpose of decreasing CHC degradation. Furthermore, the material used is not hydrogen, but rather silane which is silicon tetrahydride (a silicon atom with four hydrogen atoms attached thereto), not hydrogen. When silane is broken up, not only does it release hydrogen, but it also releases silicon which could be a contaminant and an undesirable byproduct.

Claims 13 and 14 depend from claim 12 and claims 22 and 23 depend from claim 21 and therefore define patentably over Mora for at least the reasons presented above with reference to claims 12 and 21.

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,

Jay M. Cantor
Reg. No. 19906
(301) 424-0355
)972) 917-5293

CLAIMS APPENDIX

The claims on appeal read as follows:

12. A semiconductor device manufactured using the following process:

providing a semiconductor device having at least one metal layer completed;

then applying a planarizing dielectric layer on top of the semiconductor device and the metal layer; and

then providing a hydrogen treatment until hydrogen diffuses throughout and substantially saturates the semiconductor device.

13. The semiconductor device of Claim 12, wherein the hydrogen treatment includes heating the semiconductor device in a hydrogen rich environment.

14. The semiconductor device of Claim 12, wherein the hydrogen treatment includes applying hydrogen in situ by introducing hydrogen as a plasma to the semiconductor device.

15. The semiconductor device of Claim 12, wherein the planarizing dielectric layer includes a first layer of TEOS, a second layer of HSQ, and a third layer of TEOS.

16. The semiconductor device of Claim 12, wherein the planarizing dielectric layer includes a first layer of TEOS applied by PECVD.

17. The semiconductor device of Claim 12, wherein the planarizing dielectric layer includes a second layer of HSQ applied by coating applied over a first layer of dielectric material.

18. The semiconductor device of Claim 12, wherein the planarizing dielectric layer includes a third layer of TEOS applied by PECVD applied over two layers of dielectric material.

19. The semiconductor device of Claim 12, wherein the semiconductor device undergoes an N_2 bake after an HSQ of a multilayer planarizing dielectric layer is added.

20. The semiconductor device of Claim 12, wherein the semiconductor device undergoes the hydrogen treatment after a final layer of the planarizing dielectric layer is added.

21. A semiconductor device manufactured using the following process:

providing a semiconductor device having thereon at least one metal layer completed; and

then providing a hydrogen treatment until hydrogen diffuses throughout and substantially saturates the semiconductor device.

22. The semiconductor device of Claim 21 wherein the hydrogen treatment includes heating the semiconductor device in a hydrogen environment.

23. The semiconductor device of Claim 21, wherein the hydrogen treatment includes applying hydrogen in situ by introducing hydrogen as a plasma to the semiconductor device.

24. The semiconductor device of Claim 21, further including a planarizing dielectric on said semiconductor device and said metal layer wherein the planarizing dielectric layer includes a first layer of TEOS, a second layer of HSQ, and a third layer of TEOS.

25. The semiconductor device of Claim 21, further including a planarizing dielectric on said semiconductor device and said metal layer wherein the planarizing dielectric layer includes a first layer of TEOS applied by PECVD.

26. The semiconductor device of Claim 21, further including a planarizing dielectric on said semiconductor device and said metal layer wherein the planarizing dielectric layer includes a second layer of HSQ applied by coating applied over a first layer of dielectric material.

27. The semiconductor device of Claim 21, wherein the planarizing dielectric layer includes a third layer of TEOS applied by PECVD applied over two layers of dielectric material.

28. The semiconductor device of Claim 21, wherein the semiconductor device undergoes an N_2 bake after an HSQ of a multilayer planarizing dielectric layer is added.

29. The semiconductor device of Claim 21, wherein the semiconductor device undergoes the hydrogen treatment after a final layer of the planarizing dielectric layer is added.

EVIDENCE APPENDIX

Not applicable

RELATED PROCEEDINGS APPENDIX

Not applicable